DDS based microwave LOs

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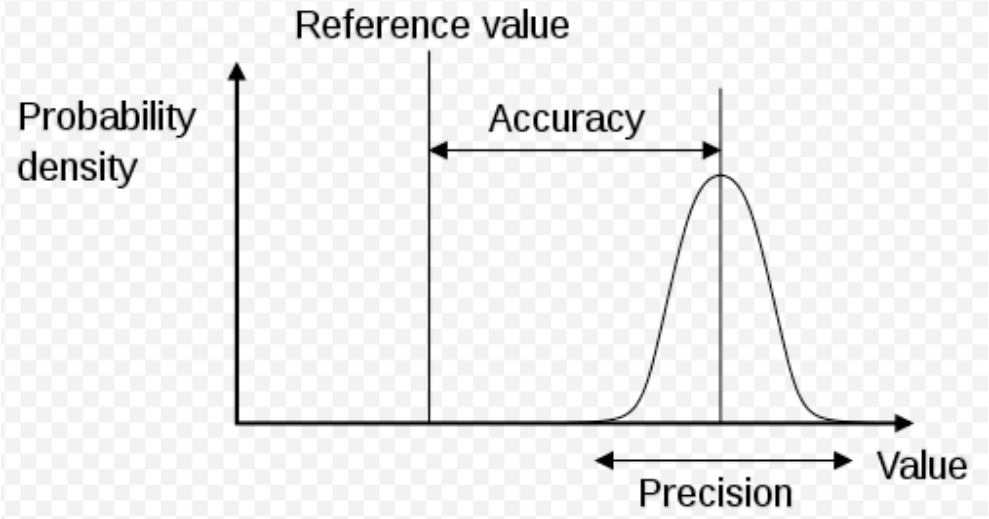
- LO requirements
- DDS performance
- Clock solution
- AD9912 real world performance
- Building an AD9912 LO setup
- The ON0GHZ 9912 Based beacon LO
- Demo and questions

LO requirements

- Frequency domain
  - Spectral purity: carrier needs to be precise
  - Spectral accuracy: carrier needs to be on-frequency
  - “phase noise” analysis
- Time domain
  - Jitter: period variability
  - Period length
  - “Allen deviation” anal.
- Today we look at frequency domain



LO requirements

- Our LO is obviously input to a mixer
- HF-VHF
  - Bad phase noise = reciprocal mixing = junk
  - Spurs are especially relevant
- Uwave and beyond
  - Bad phase noise/stability = absence of coherence = inability to detect signal
  - Even without spurs RF noise mixes and degrades NF, at high multiplication factors

LO requirements

- How good is a good LO?
  - For a spur it is easy to compute how the reciprocal mixing influences RX
  - In a much cleaner environment… how much phase noise do we need… simple approach
  - IF BW 100Hz, RX BW sys 100MHz (pipe caps), thermal noise doubles if LO noise floor *-60dBc/Hz at 10GHz, safe at -70dBc/Hz*
  - WA1ZMS says commercially -90dBc/Hz is used

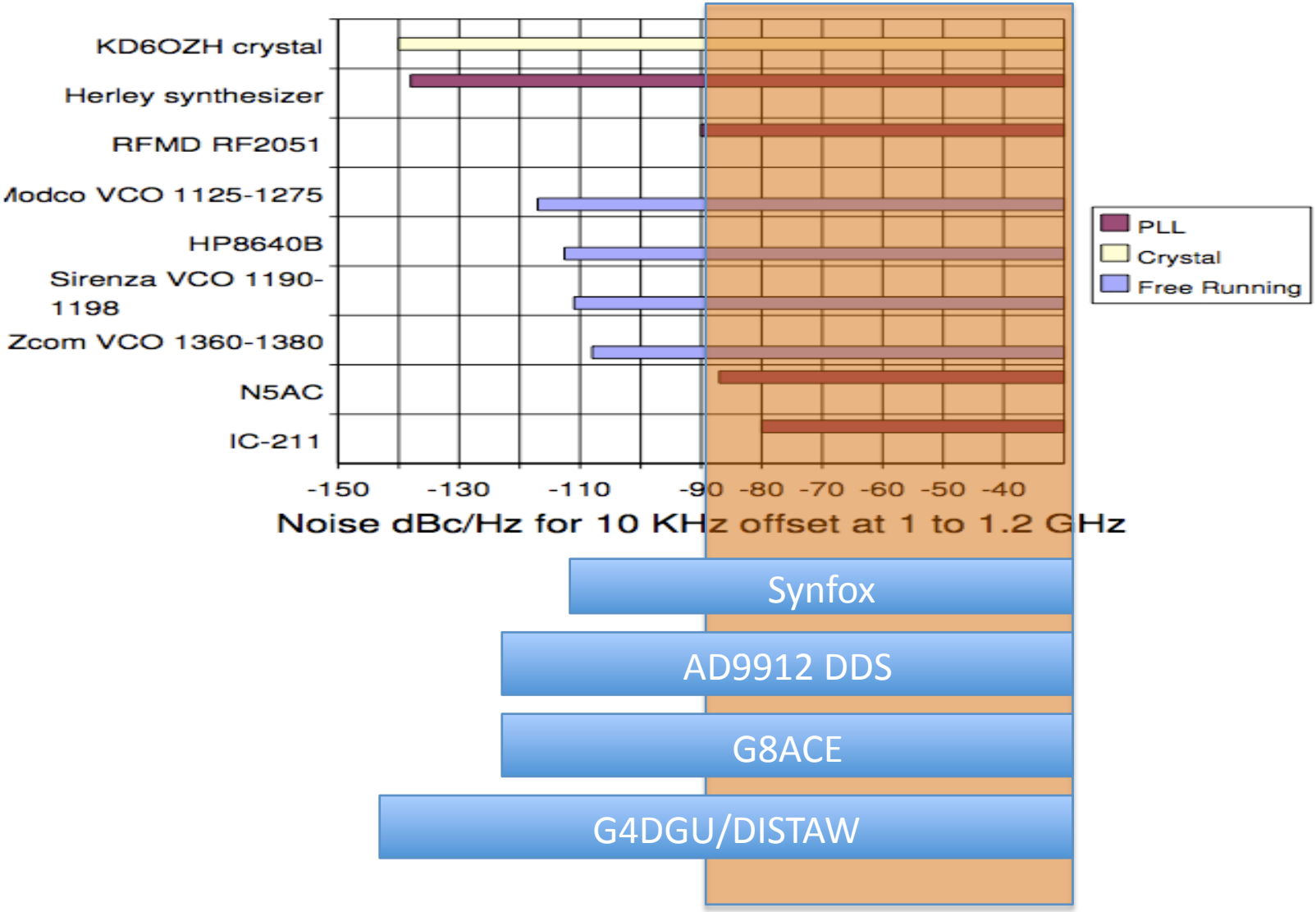
LO requirements

- How good is a good LO (2)?
  - Multiplication *N rule: 20logN
  - AM noise
  - So noise floor at 1GHz: -90dBc/Hz min
  - So noise floor at 100MHz: -110dBc/Hz min
  - Alternatively: IF 100Hz, RX sys 10KHz, @10KHz: -20dBc/Hz, safe -30dbc/Hz, 1GHz: -50dBc/Hz@, 100MHz: -70dBc/Hz
  - On 47/76GHz: we need another 14/18dB

JT4/QRSS

- New modes for weak signals on uwave
- JT4A… BW is 17.5Hz, S/N limit -23dB
- QRSS 1Hz BW
- If we disregard spreading on uwaves
- 1Hz BW means -90dBc/Hz @10kHz needed on 1GHz for a QSO on 100GHz
  - “many” solutions no longer acceptable
  - reality must be better

Some measurements by K0CQ



More comparisons

- Close-in XOs are still better @1KHz, 1GHz
  - G8ACE -111 dBC/Hz
  - G4DGU DISTAW -125
  - “pure” AD9912 -109
  - locked AD9912 -104

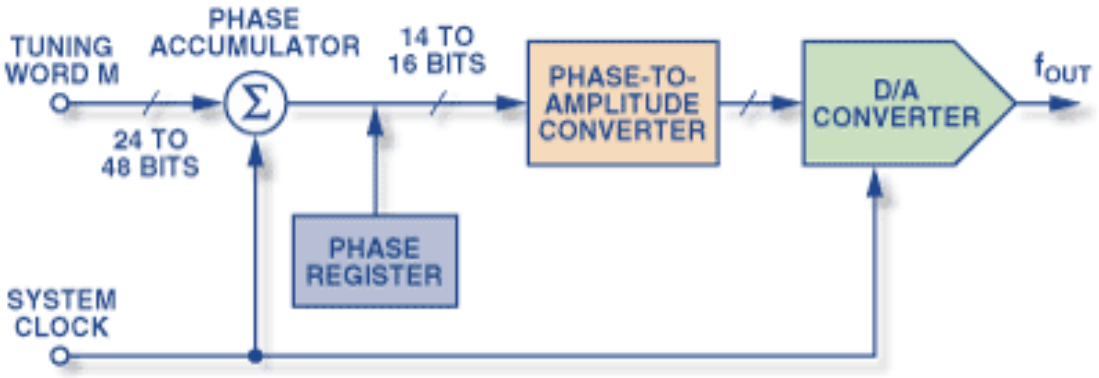
  - All in the “good zone”

A good LO

- PN: @1kHz: -100dBc/Hz, @10KHz: -110dBc/Hz, floor -140dBc/Hz for an 100MHz oscillator will keeps us out of trouble up to 100GHz
- locked to stable references so accurate
- next some system requirements:
  - Cheap
  - Agile
  - Easy, …

DDS as LO

- DDS principle
- http://www.analog.com/library/analogDialogue/archives/38-08/dds.html
- DDS = clock divider



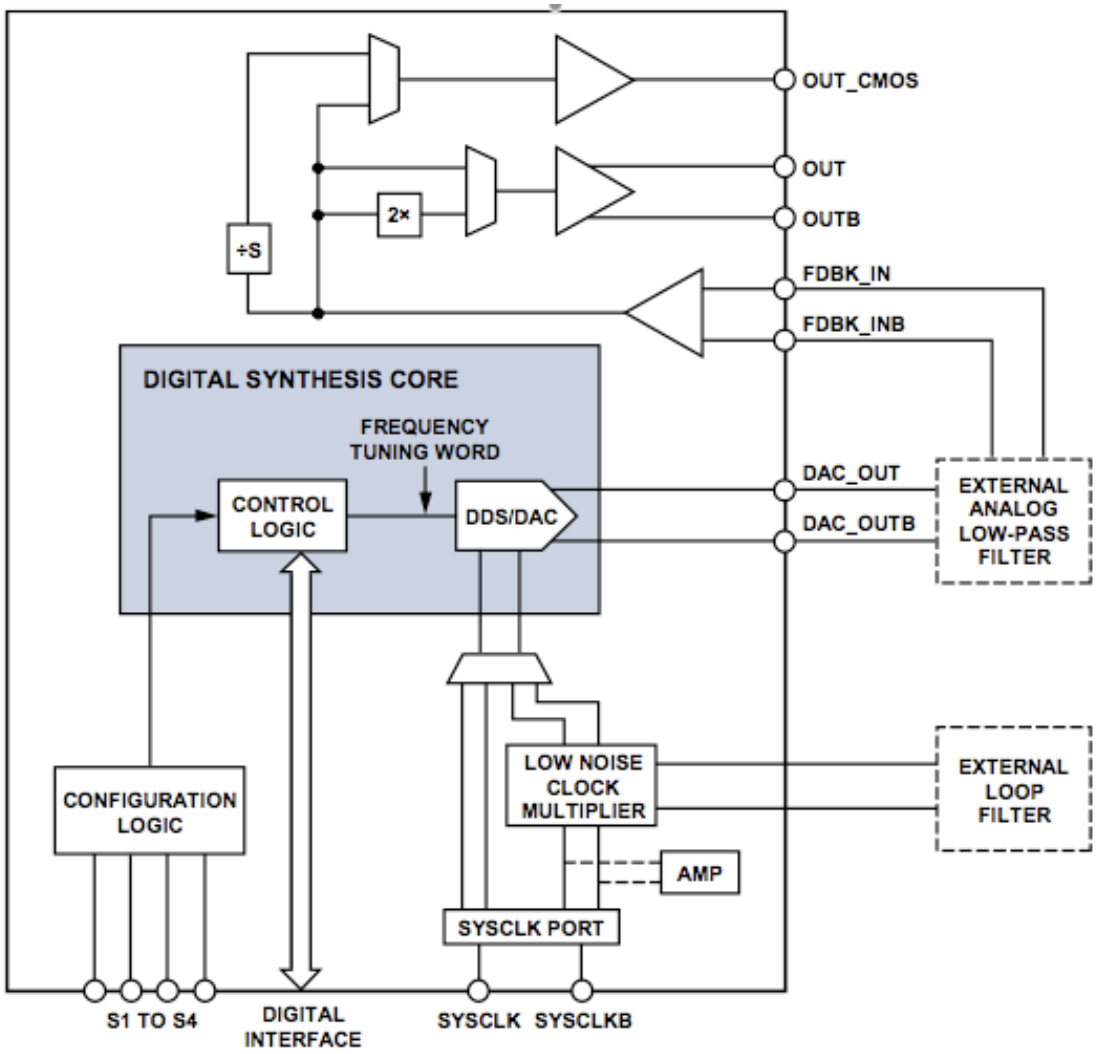
DDS performance

- Spurs
  - Clock spurs (improved)
  - Phase truncation
  - Phase / amplitude errors
  - DAC errors
- Noise
  - AM / PM
  - DAC
  - Clock

Enter the AD9912

- Until now spurs and PN too big for uwave LOs
- AD9912
- “DDS is so good that only clock is relevant”
  - 48 bit tuning word
  - 14 bits DAC
  - 1GHz clock !
  - SFDR +/- 250KHz -95dB
  - Only <1W DC
  - 50 EUR DigiKey or sample

AD reference design



AD9912 LO

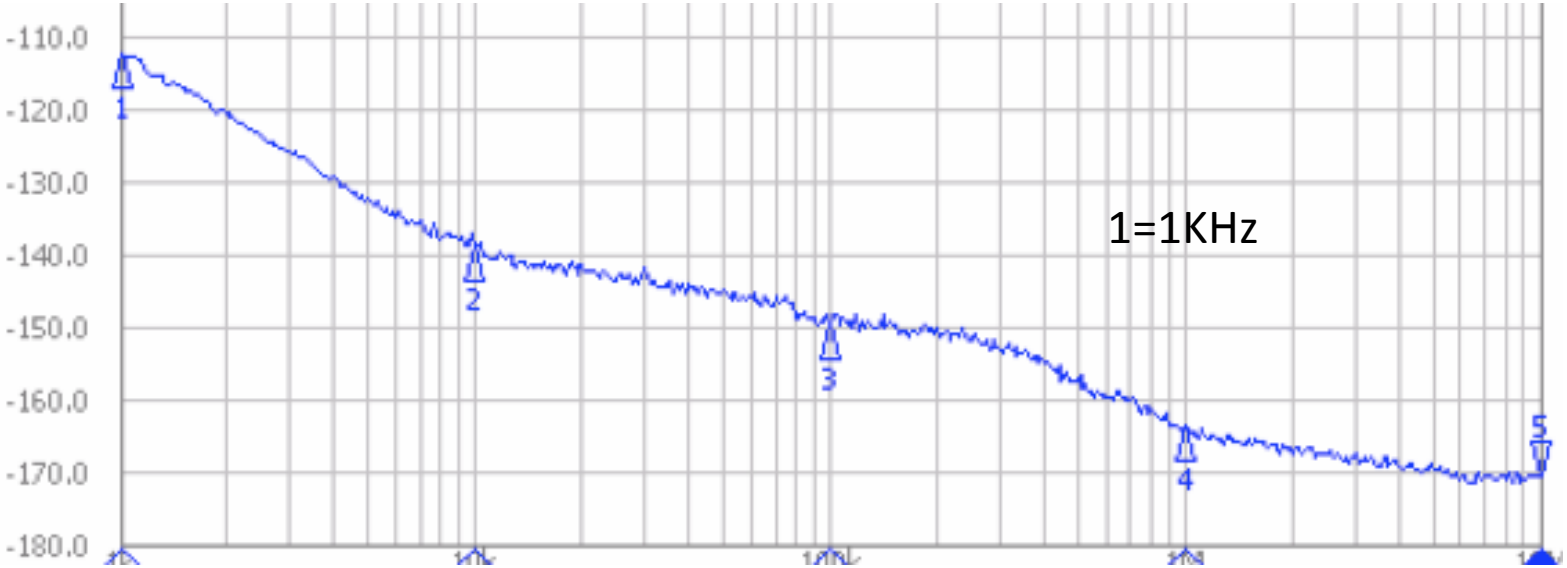
- Agile: only need 1 instead of Xtal based LOs (13, 6, 3, 1.2 …)
- No need for quality Xtals
- No tune
- uP controlled switching
- Easy to lock
- … The problem reduces to a locked clock design

A good quality LOCKED clock

- … on 1GHz
- Some approaches
  - 10 MHz + multiply * 100
  - 10 MHz locks 100MHz VCXO + * 10
  - 10 MHz locks wideband VC resonator at 1GHz for example Si571
  - 10 MHz locks narrowband VC resonator at 1GHz for example Crystek 55CX1000-1000

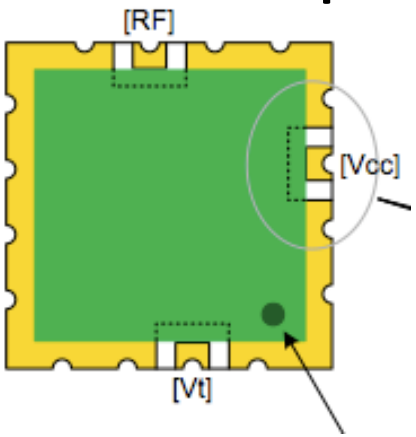
Crystek VC-CRO

Crystek Part Number	Frequency (MHz)	Phase Noise @ 10kHz Typ (dBc/Hz)	Tuning Voltage (Vdc)	Kvco (MHz/V)
CVCO55CX-1000-1000	1000 to 1000	-135	0 to 5	1



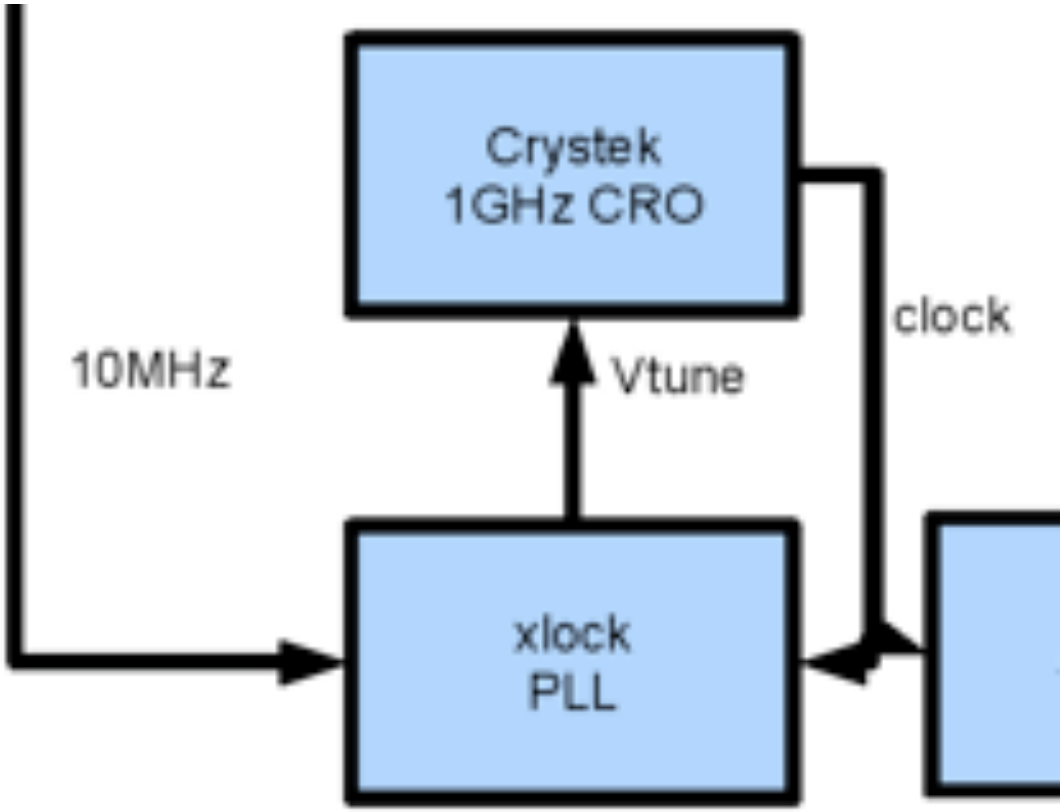
Crystek VC-CRO (2)

- Cheap - < 50 EUR in small quantities
- Simple
- Output 10dBm



- All that remains to be solved is the lock
- … I like using the PLL chips LMX/ADF

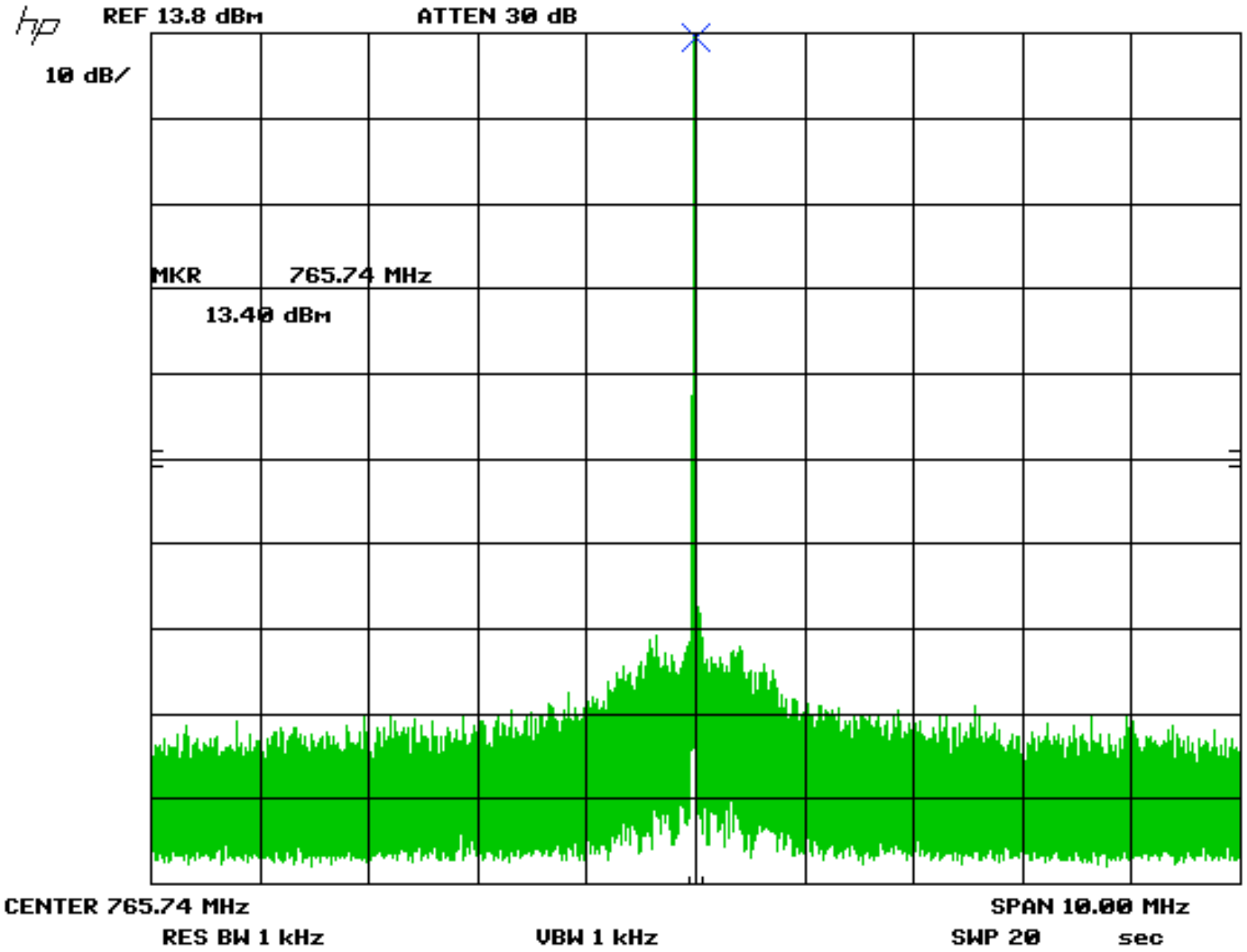
The locked clock

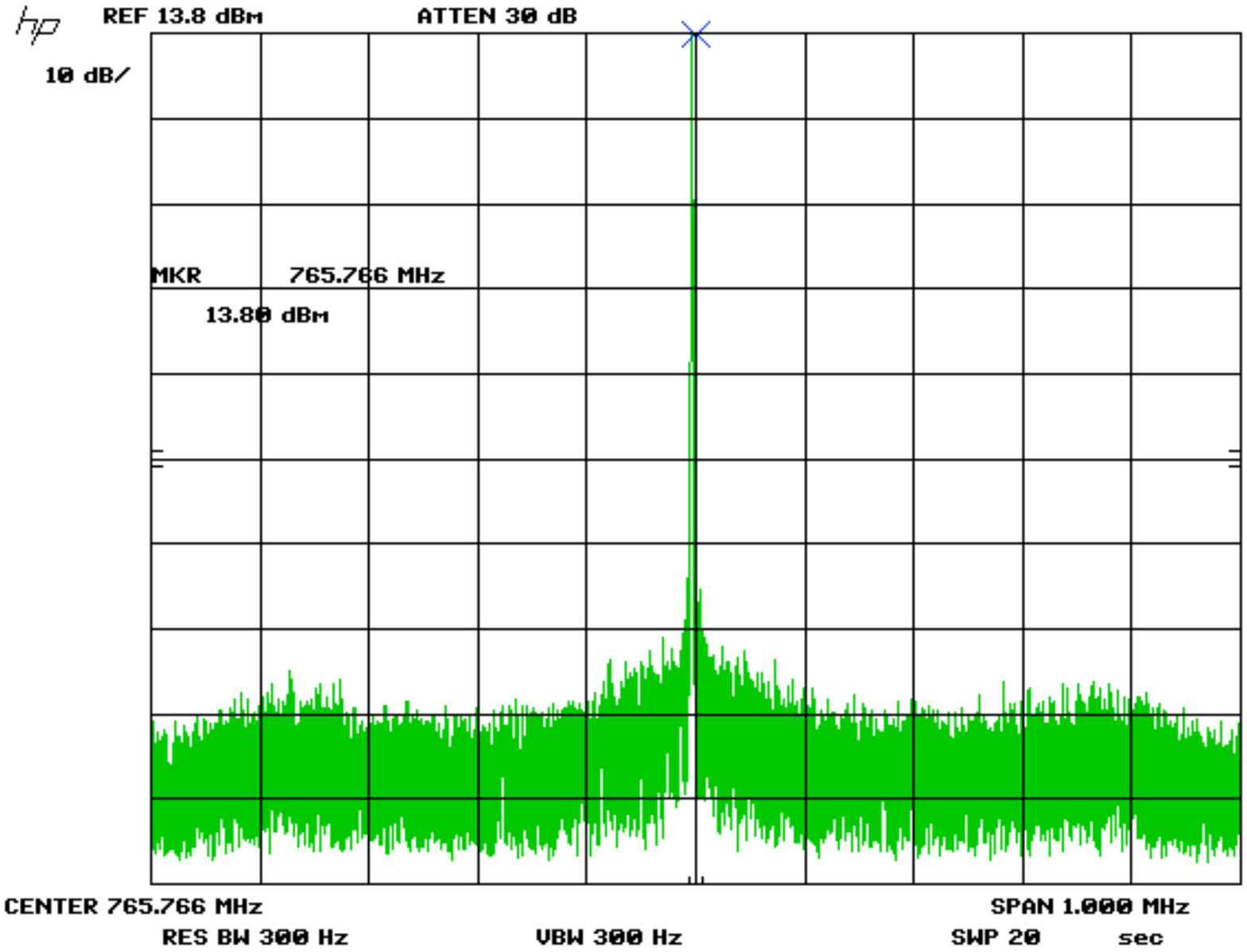


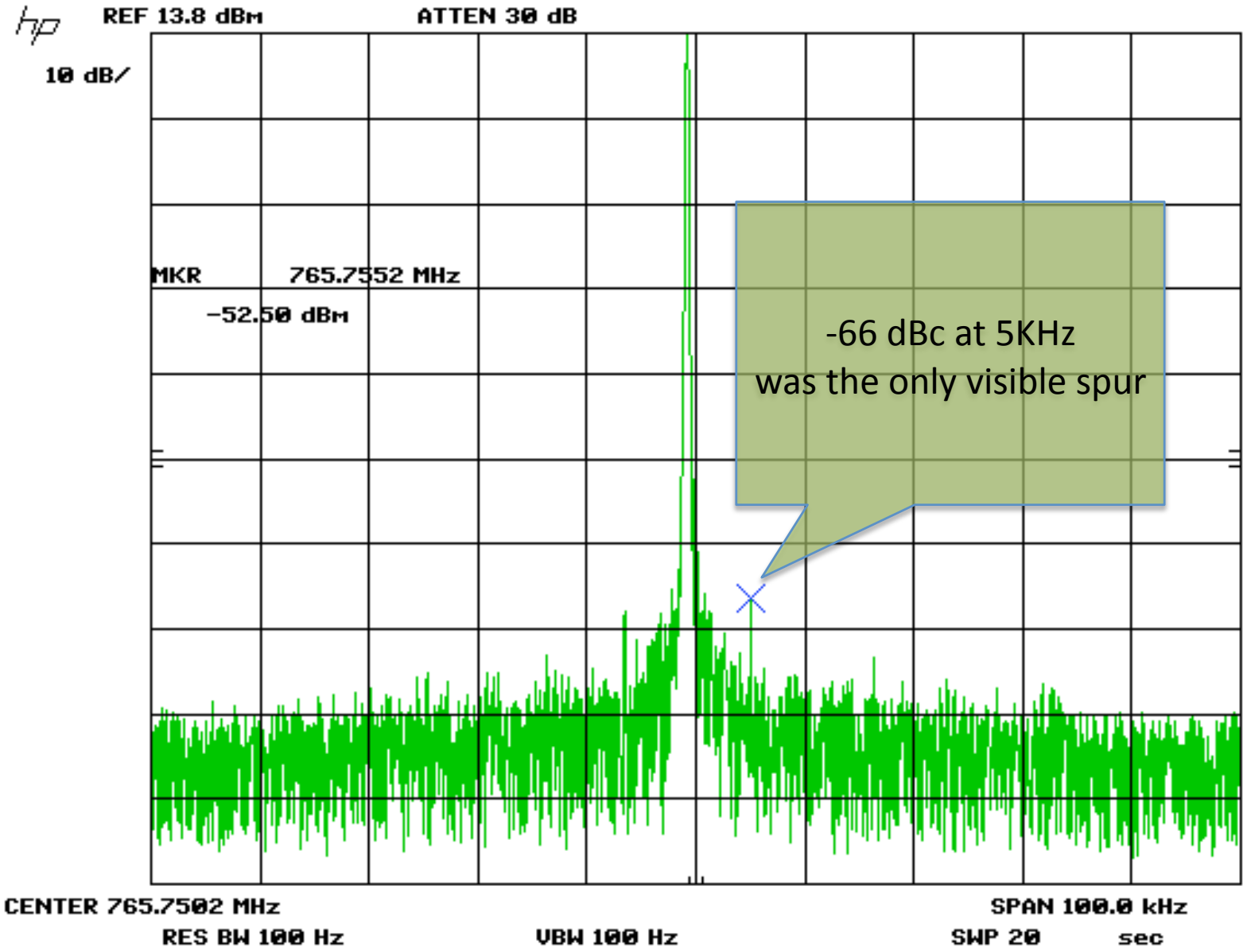
- Xlock PLL design presented at CJ2007

Real world performance - spurs

- Multiply AD LO output to 10GHz using db6nt
- Mix down to < 1GHz
  - HP 11729C carrier noise test set
  - HP 8662A low phase noise synth
  - 10368MHz – 640MHz * 15 = 768 MHz
  - Using ultra clean 640MHz from HP 8662A
  - Look at spectrum on HP 8568B analyser

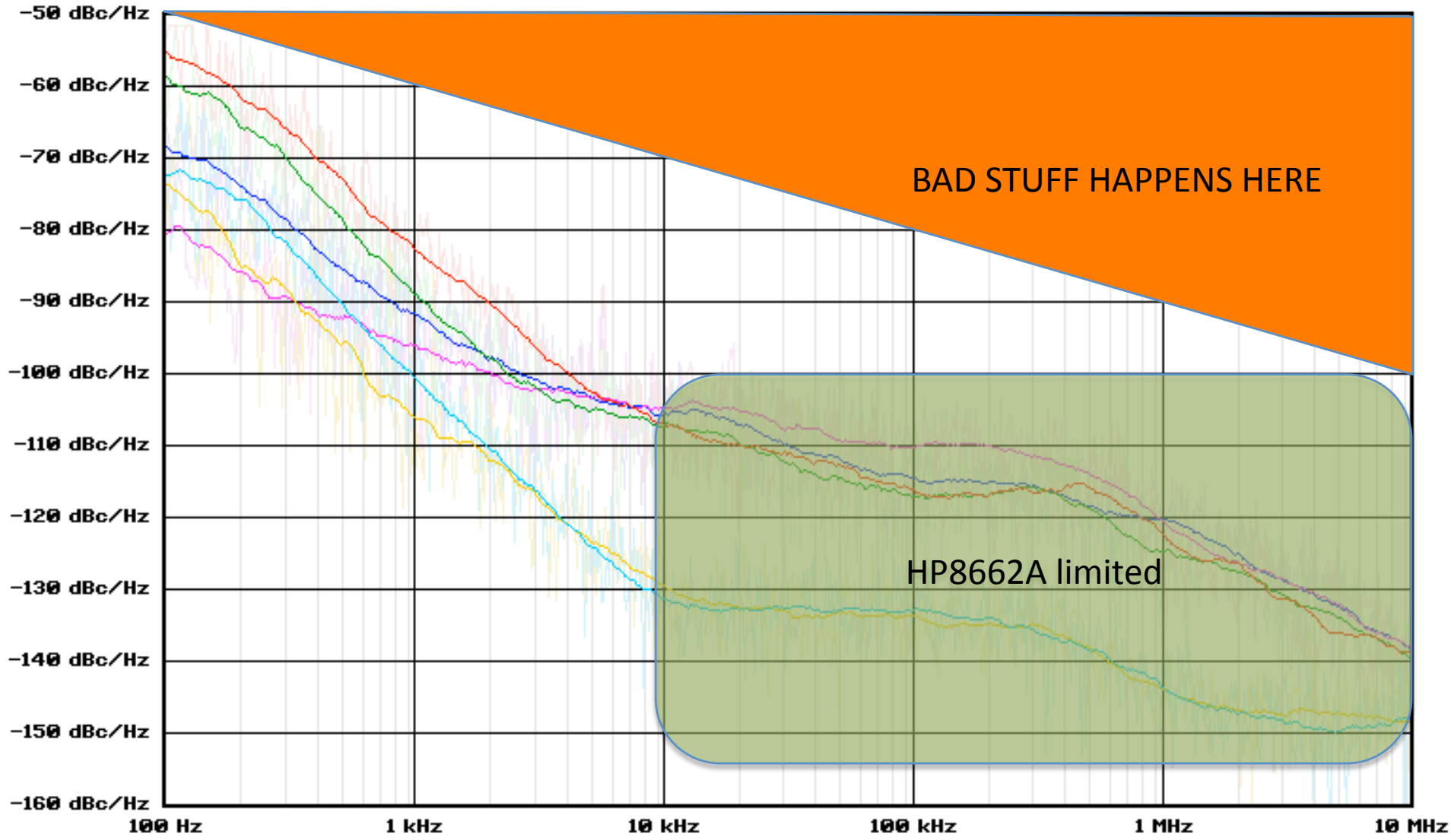

REF 13.8 dBm
ATTEN 30 dB
10 dB/
MKR
765.74 MHz
13.40 dBm
CENTER 765.74 MHz
SPAN 10.00 MHz
RES BW 1 kHz
VBW 1 kHz
SWP 20 sec


hp
REF 13.8 dBm
ATTEN 30 dB
10 dB/
MKR
765.766 MHz
13.80 dBm
CENTER 765.766 MHz
SPAN 1.000 MHz
RES BW 300 Hz
VBW 300 Hz
SWP 20 sec


REF 13.8 dBm
ATTEN 30 dB
10 dB/
MKR
765.7552 MHz
-52.50 dBm
-66 dBc at 5KHz
was the only visible spur
CENTER 765.7502 MHz
SPAN 100.0 kHz
RES BW 100 Hz
VBW 100 Hz
SWP 20 sec

Real world performance - PN

- Multiply AD LO output to 10GHz using db6nt
- Measure phase noise on 10GHz
  - HP 11729C carrier noise test set
  - HP 8662A low phase noise synth reference source
  - various LO measured: G8ACE, 8662A-2, AD9912, AD9912 locked, 1GHz clocks from Crystek
- http://www.ke5fx.com/HP_PN_seminar.pdf



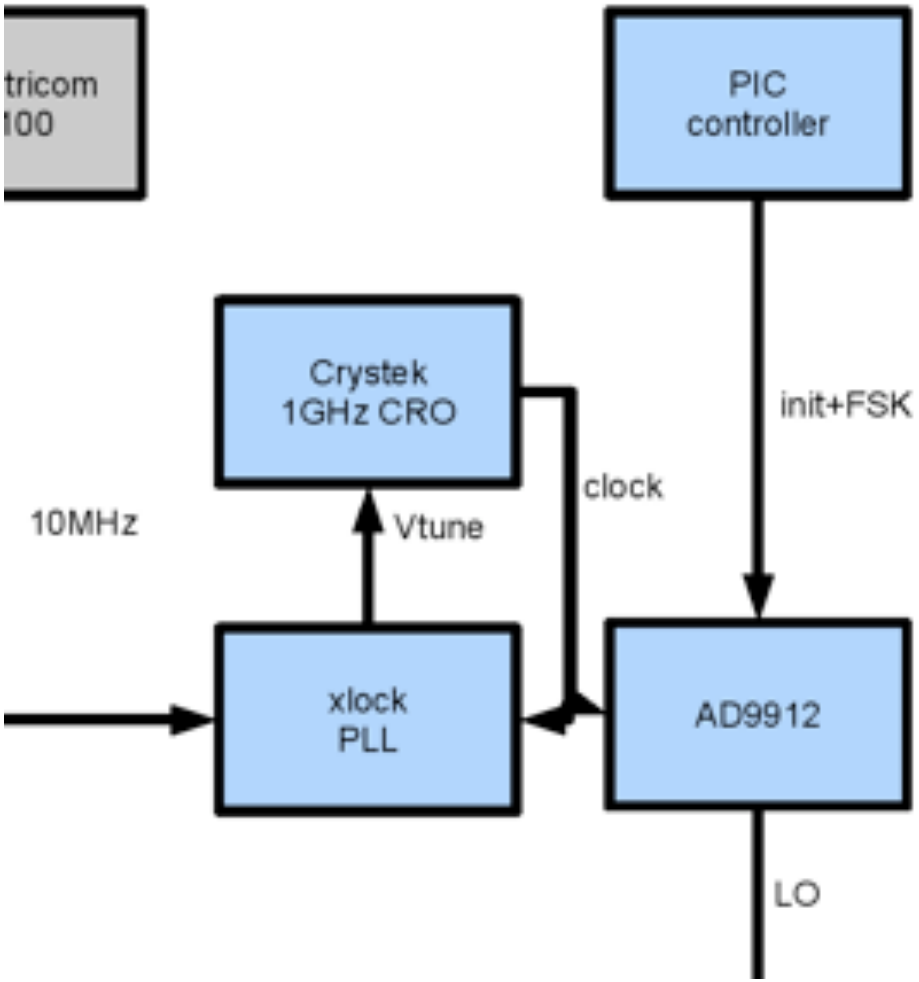
Trace	Carrier Hz	Carrier dBm	dBc/Hz at 100 Hz	RF Atten dB	Instrument
10G BCN -- G8ACE	10 368 975 000	-7.00	-68.5	10	HP8568B
10G BCN -- AD9912 -- 8662A -- 1dbm2	10 368 975 000	-7.00	-80.6	10	HP8568B
10G BCN--9912-CVCO-11729--100	10 368 975 000	-7.00	-58.9	10	HP8568B
10G BCN--AD9912--CVCO-lock-11729--100	10 368 975 000	-7.00	-55.4	10	HP8568B
1GHZ-CVCO-11729--100	1 000 000 000	-7.00	-73.6	10	HP8568B
1GHZ-CVCO-lock-11729--10	1 000 000 000	-6.60	-72.4	10	HP8568B

Improvements

- Currently LMX2306 is used in clock PLL
- Very narrow loop 50Hz
- Outside loop CRO noise takes over
- Solution: wider loop
- … very fast loops need good phase comparators in PLL that are not noisy
- ADF4107: 12dB better and R=1, not 3 (8db)
- At 1KHz we can gain 20dB PN if our reference is sufficiently clean on 10MHz (HP 3801, Thunderbolt)

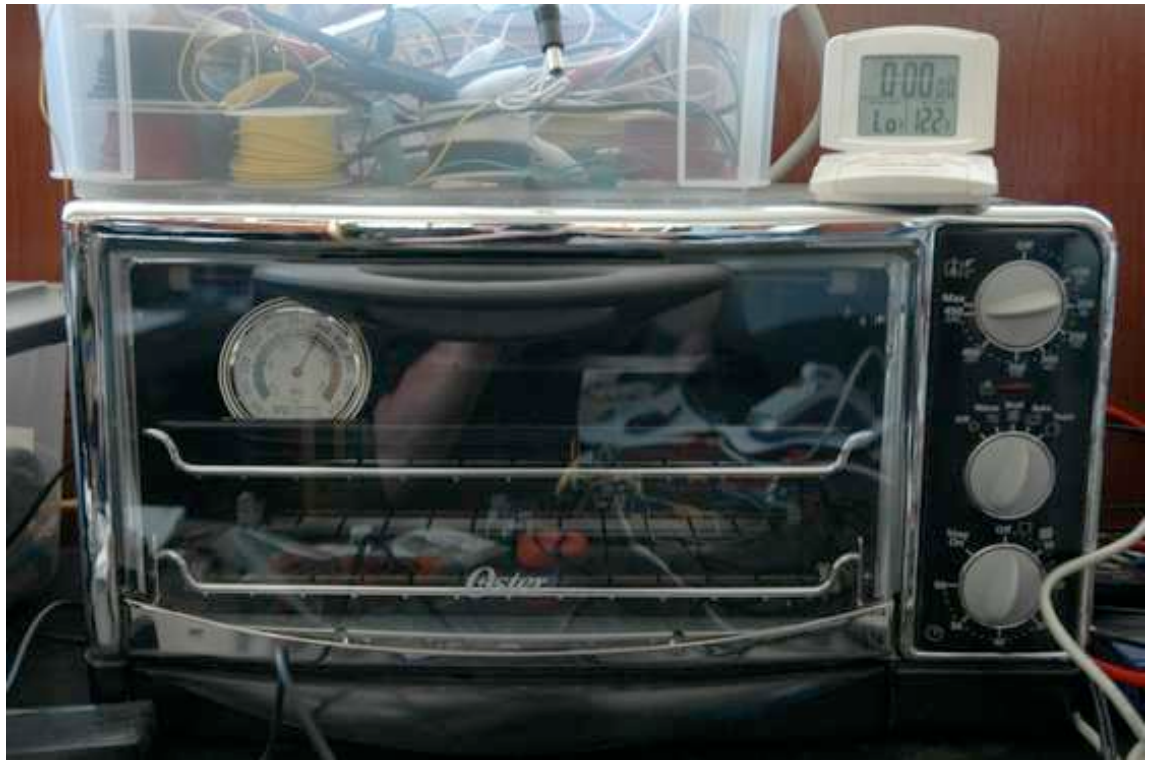
Putting it all together

- PIC 1 controls AD9912
  - Init AD chip
  - Change frequency
- PIC 2 controls PLL
  - Init LMX/ADF
  - Watch lock

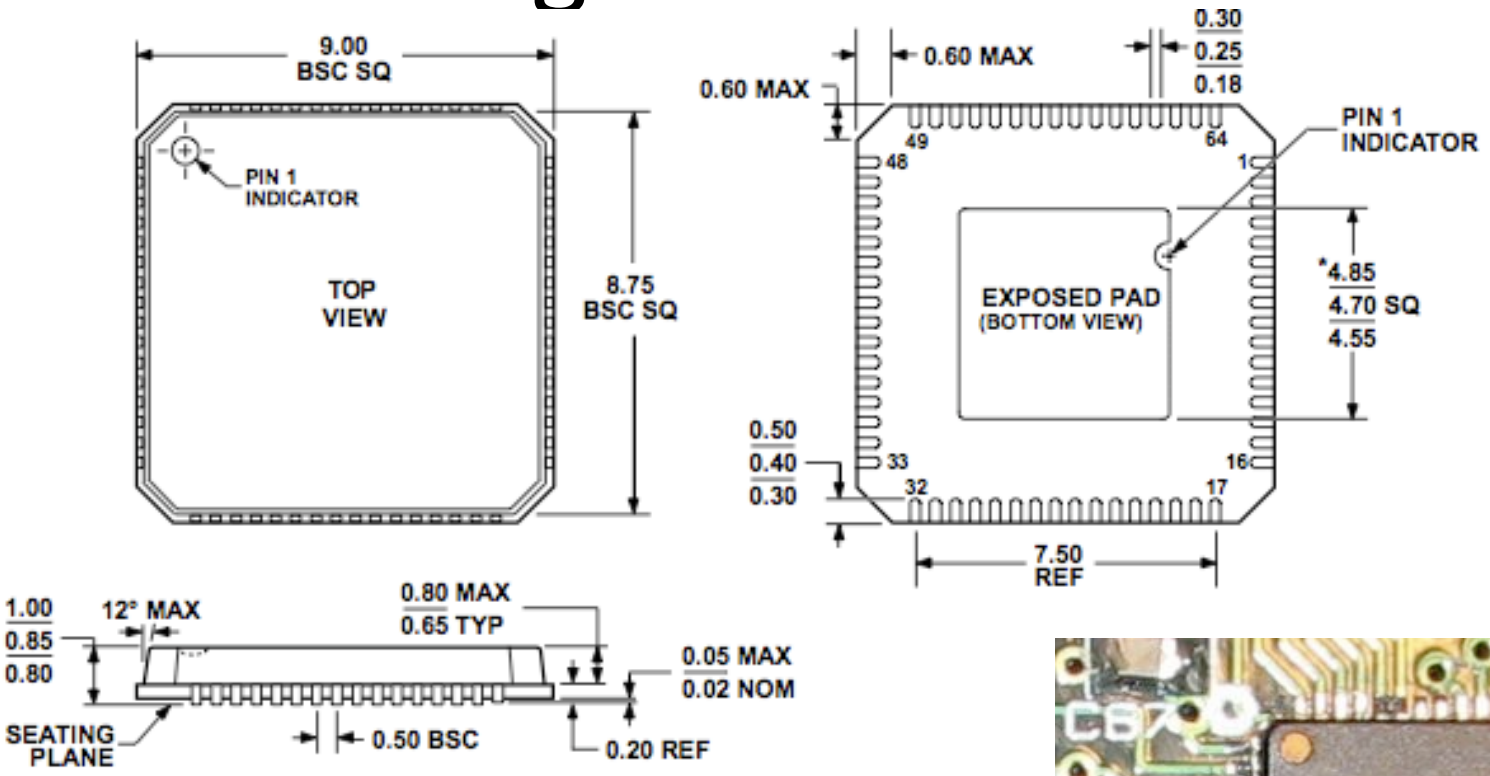


Building the DDS based LO

- Most important tools



Building the DDS based LO

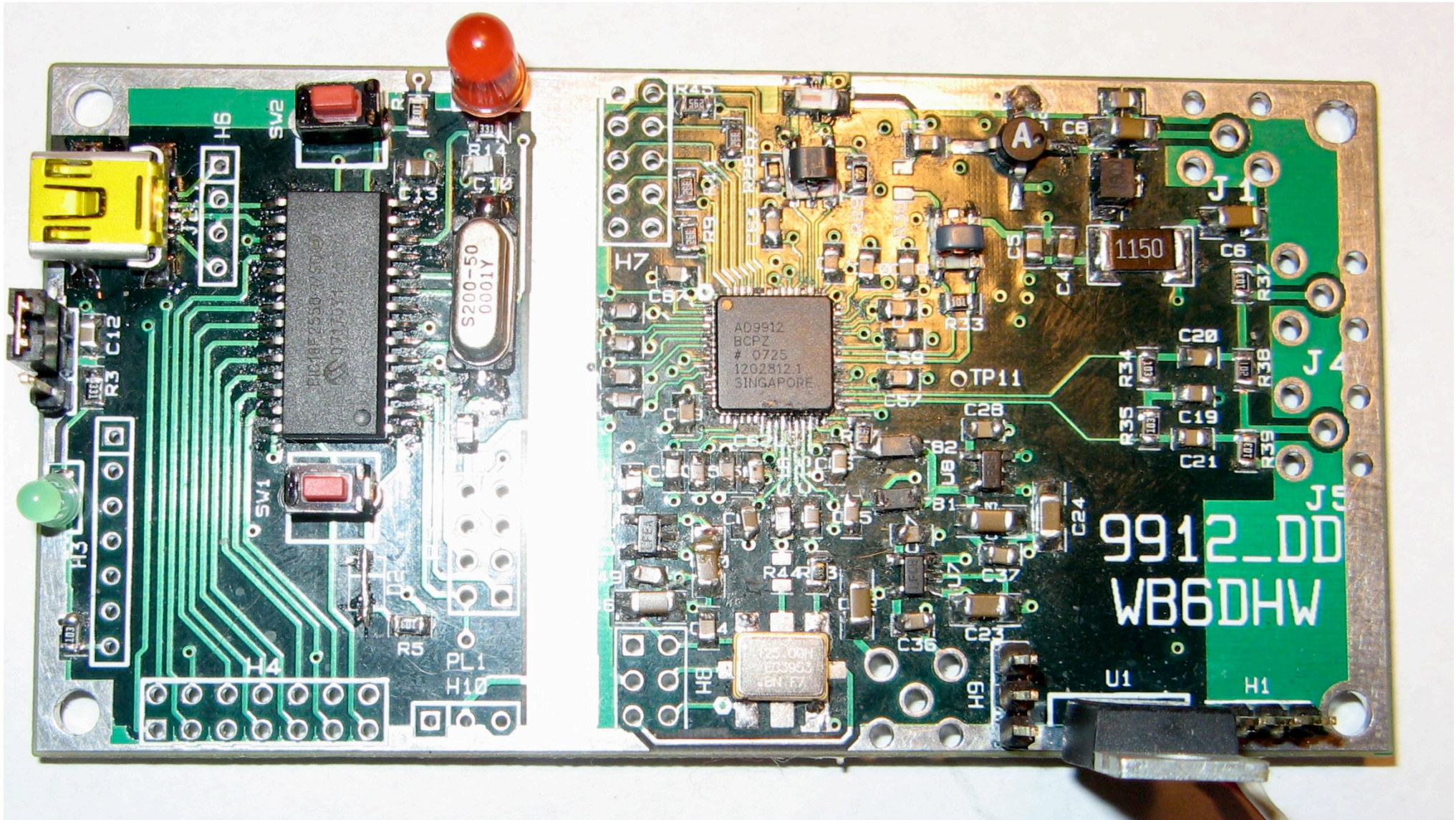


*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD
EXCEPT FOR EXPOSED PAD DIMENSION

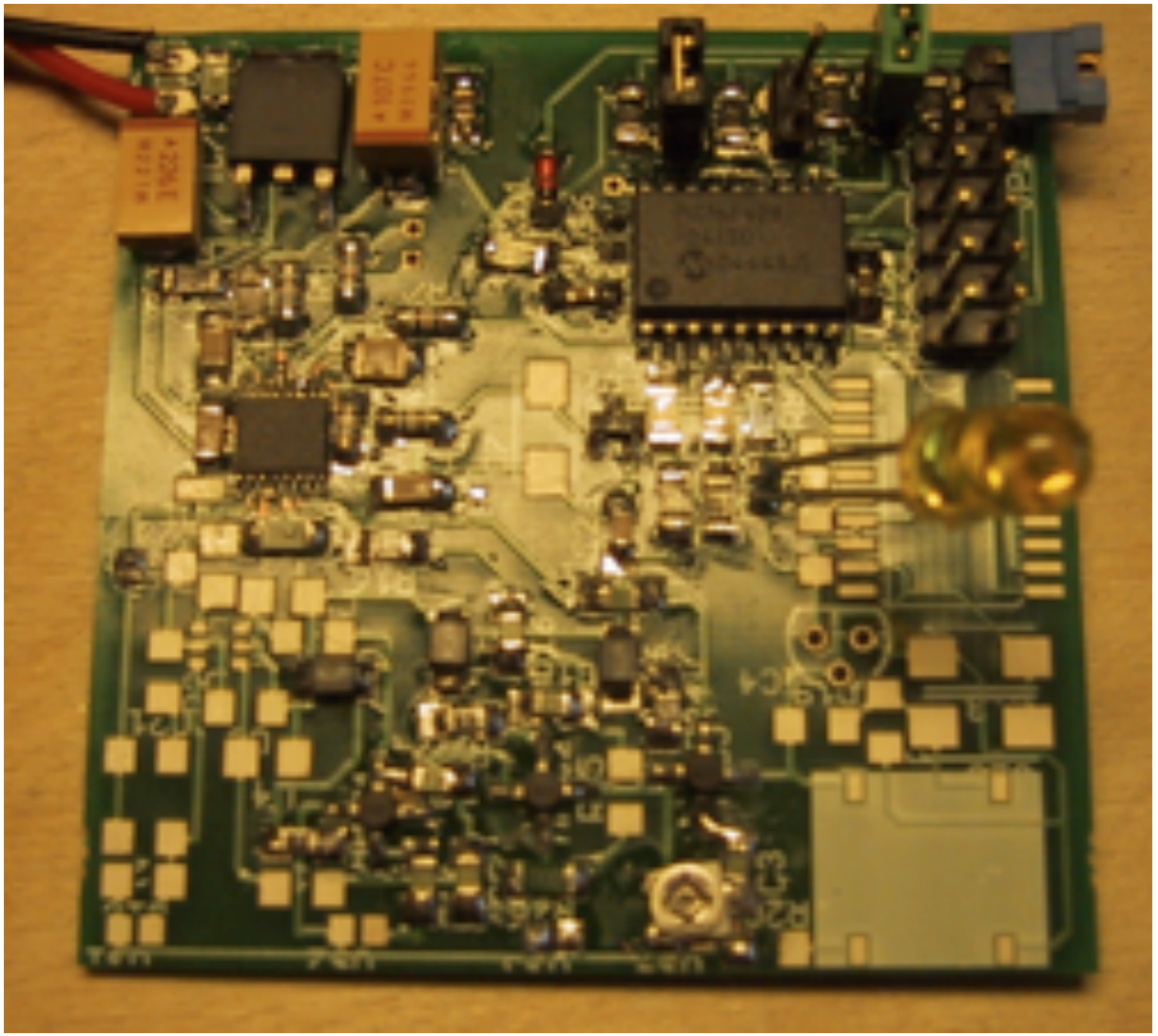
Figure 57. 64-Lead Lead Frame Chip Scale Package [L
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

Building the DDS based LO

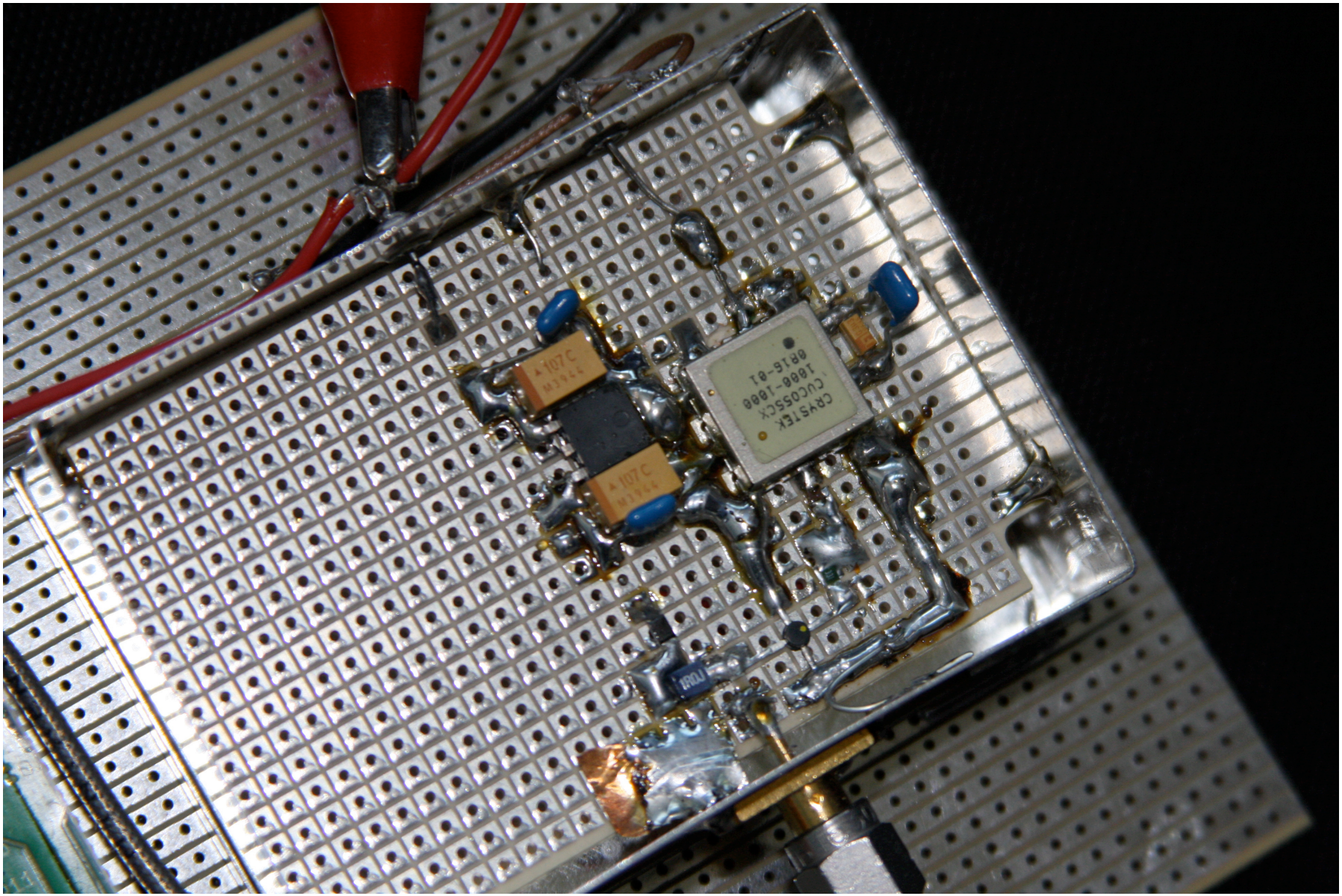
WB6DWH 4 layer – reference application

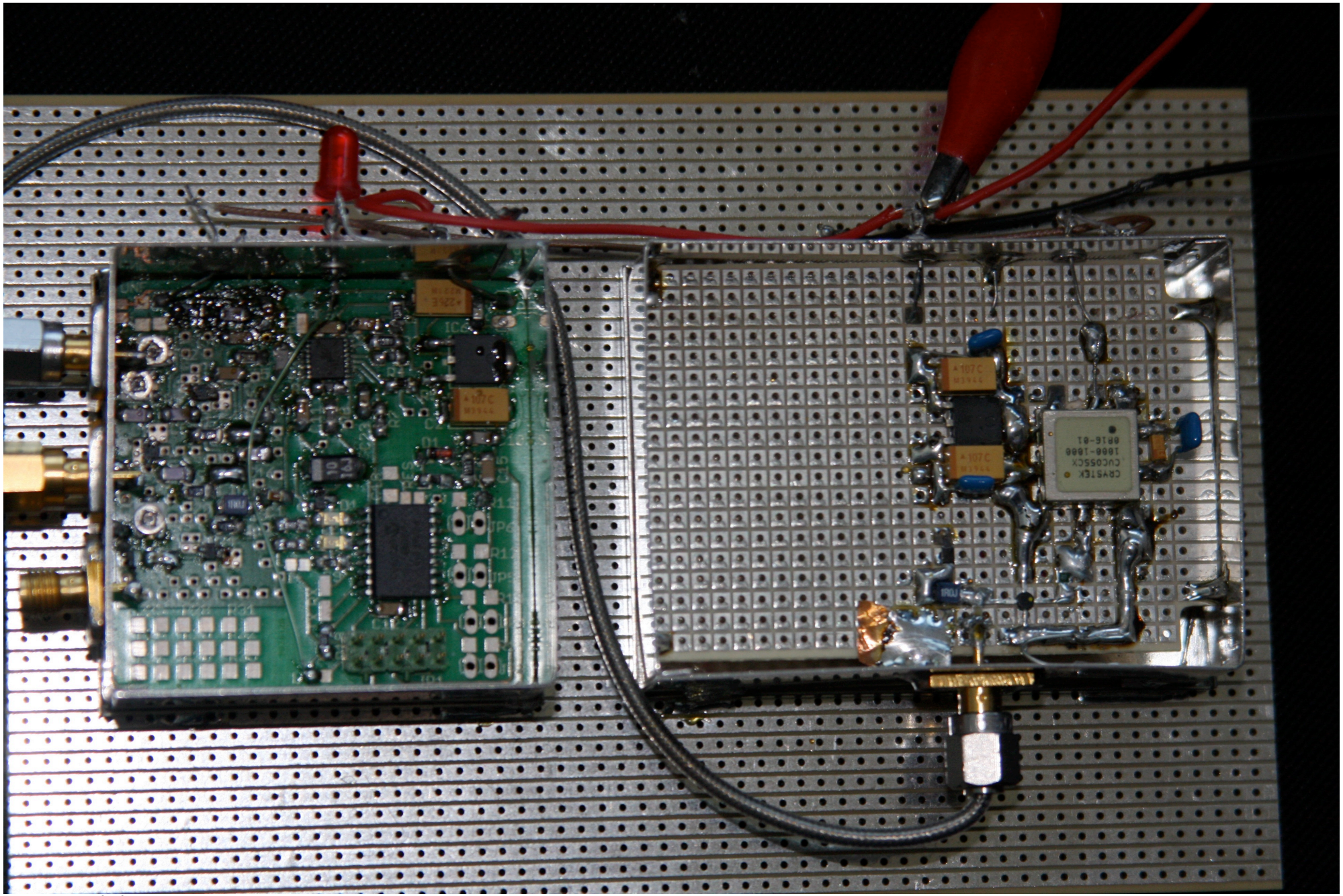


The 1 GHz clock PLL



1GHz clock





Programming the AD9912

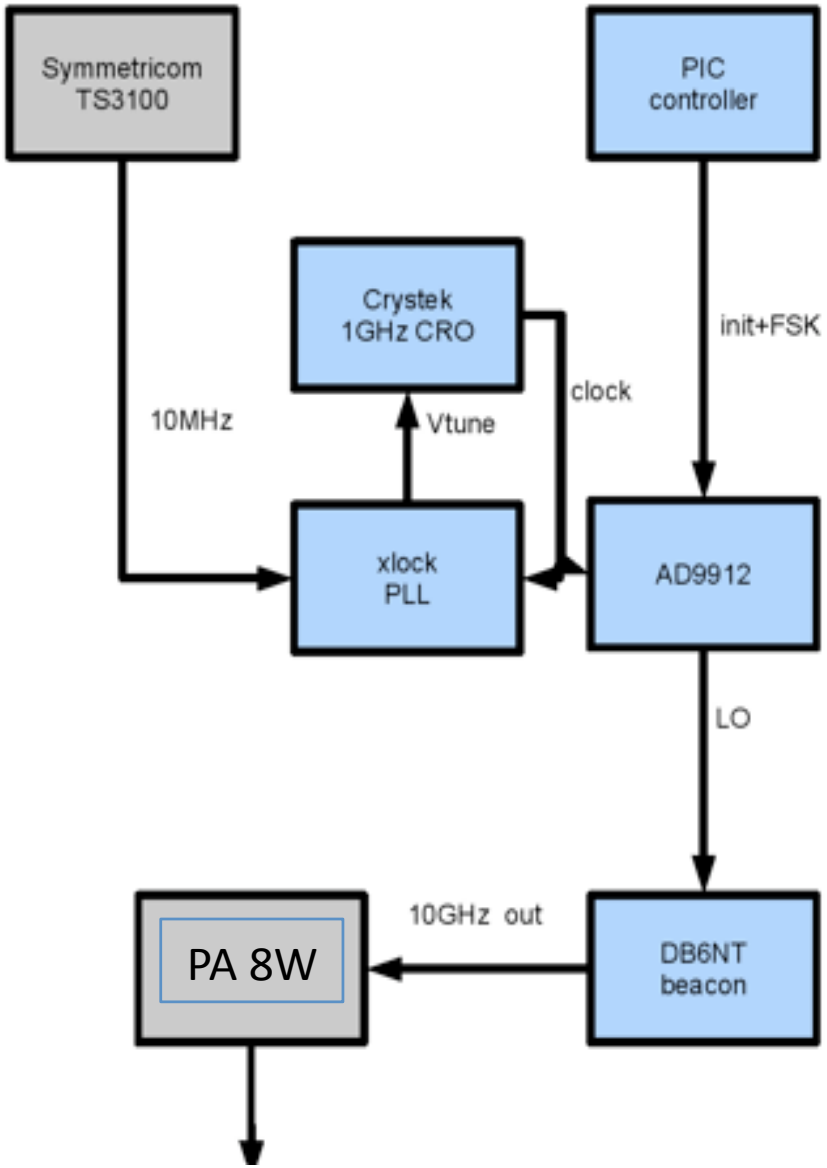
- Very simple
  - Init();
  - Set_FTW();
- Serial 2 wire interface: clock and data
- Chip Select
- Just a matter of PIC PIN magic
- For our application, FTW calculation on other CPU (48 bit math is complex)

Programming ctd.

- PIC18F2550 USB
- Boot loader
- In field programming using USB
- Programming in Microchip C
- Possibility for in/out using USB/serial framework
- Currently: set fixed frequency and FSK code
- Other code available - standalone

First application 3cm ON0GHZ/B

- Calculate FTW for Mark and Space
- PIC provides M/S to DDS
- Very simple to achieve locked beacon
- Demo CJ 2009, 10.368.975 MHz, 23dBm
- (24GHz ON4CDU locked operational 4/09)



Wrap - up

- Demo
- Questions
- Thanks!
- xtof@cs.kuleuven.be
- xtof@huygens.biz